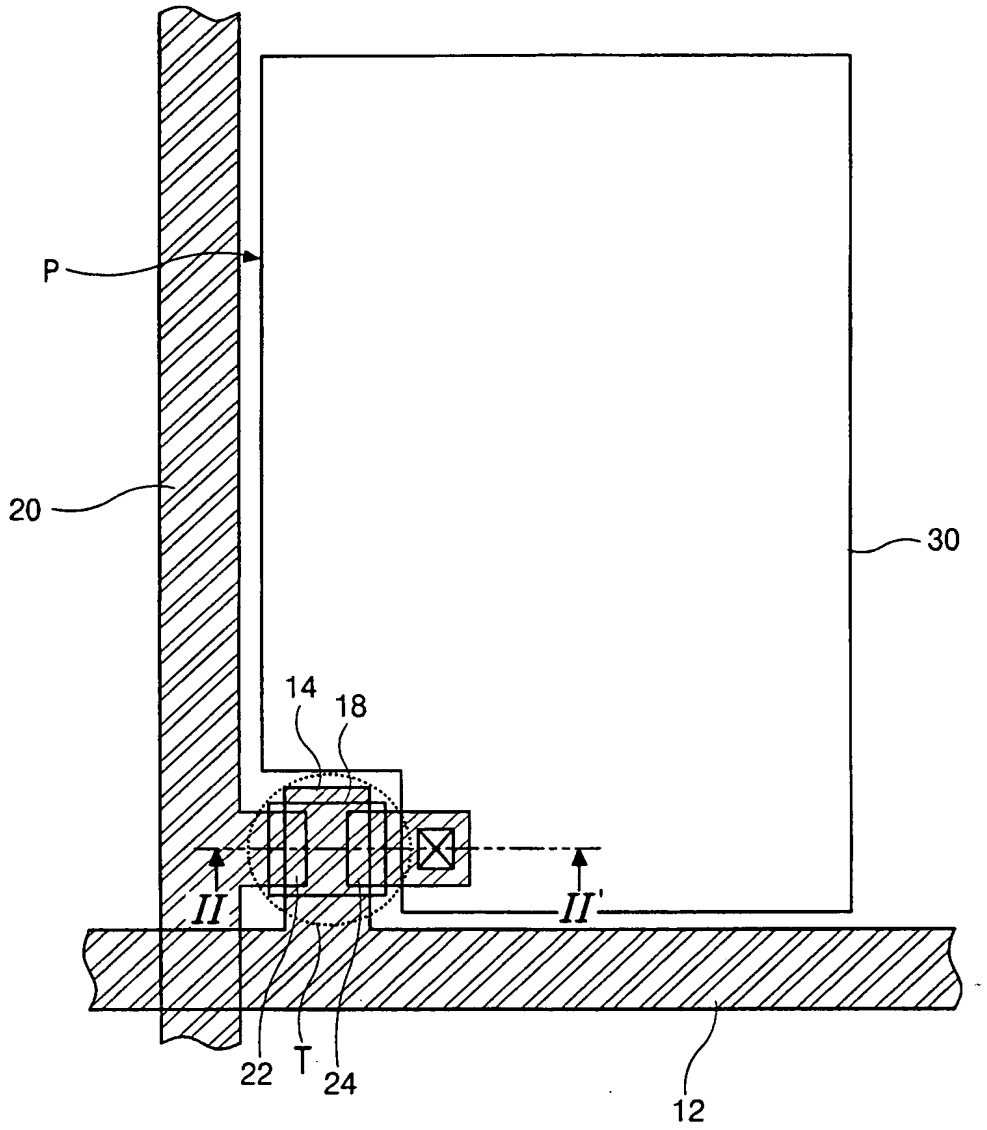

FIG. 1A
RELATED ART

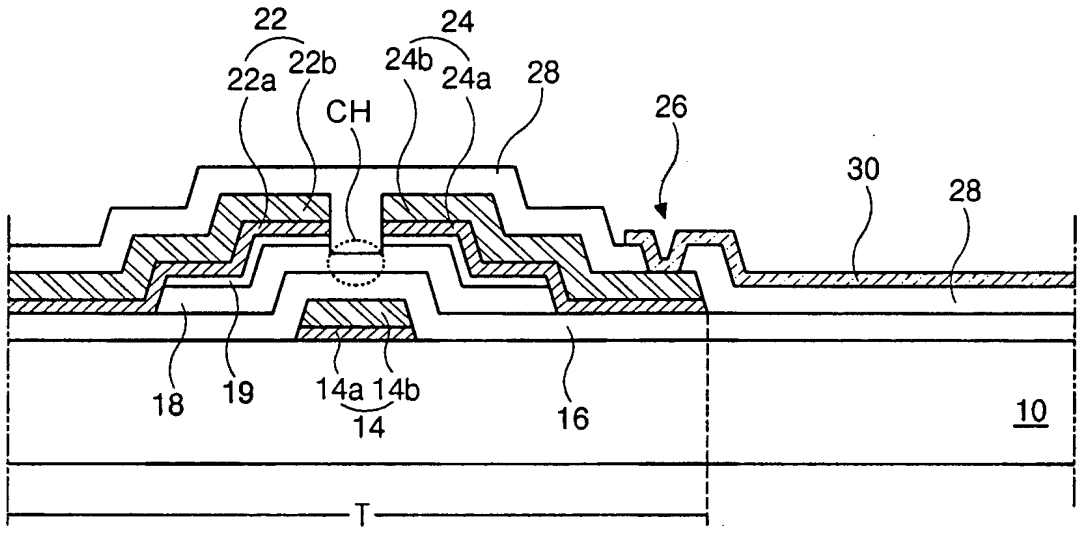

FIG. 1B
RELATED ART

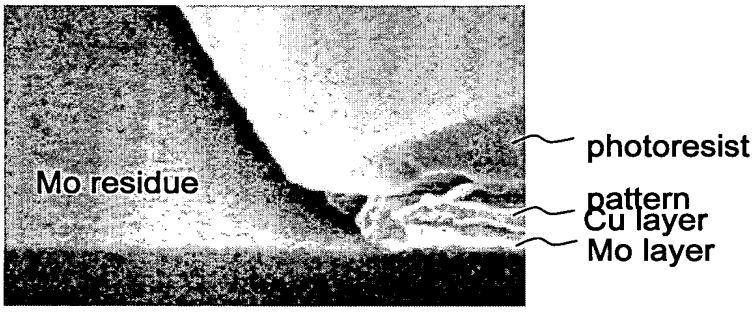

FIG. 2A
RELATED ART

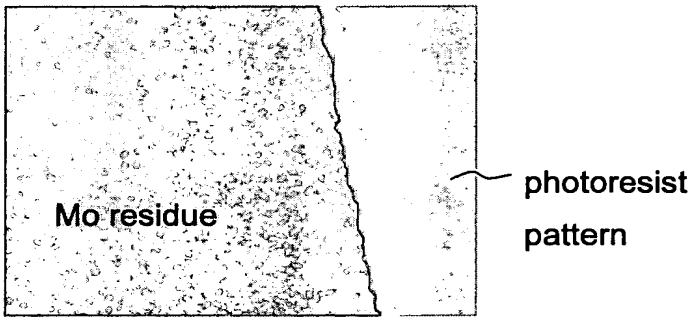

FIG. 2B
RELATED ART

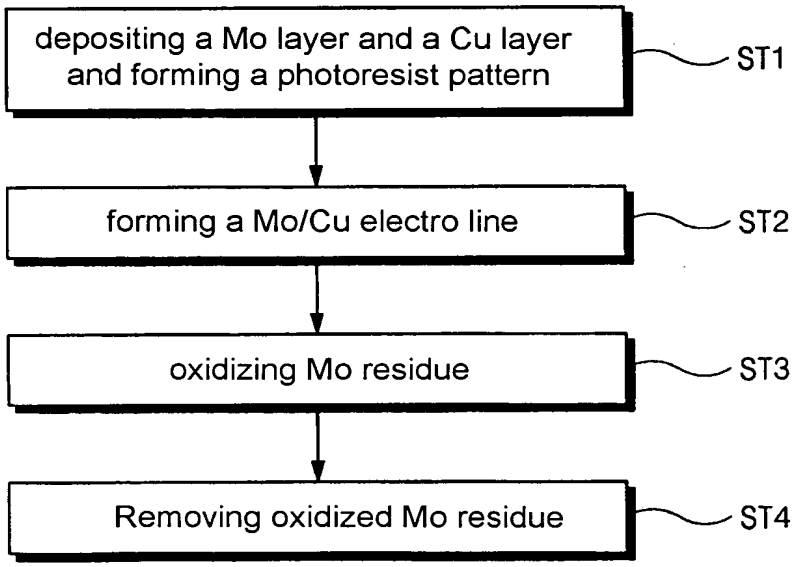

FIG. 3

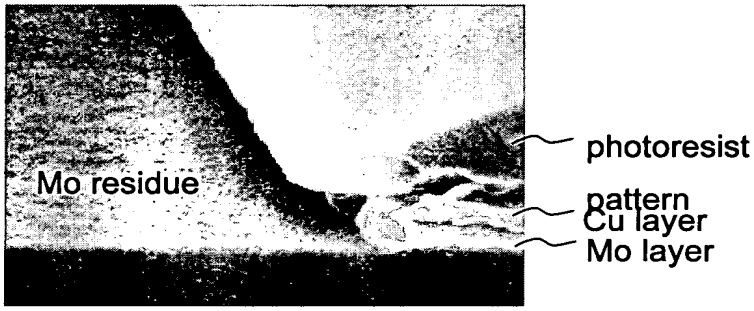

FIG. 4A

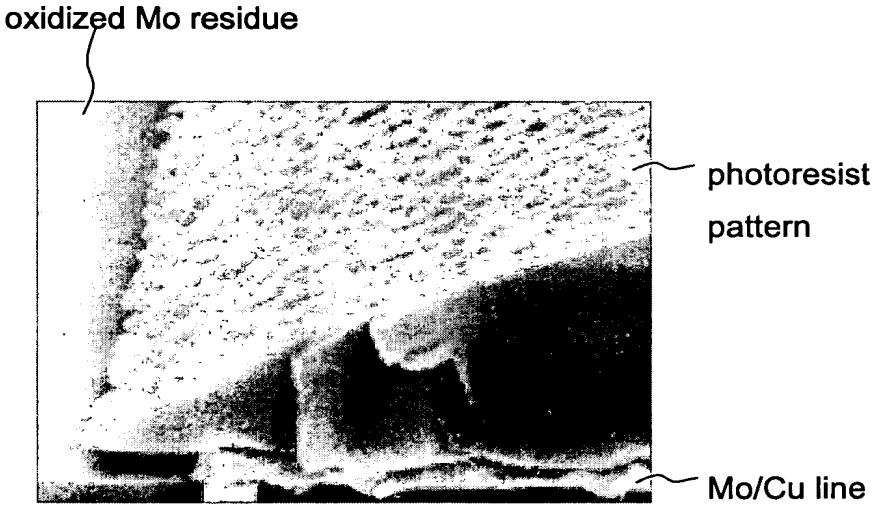

FIG. 4B

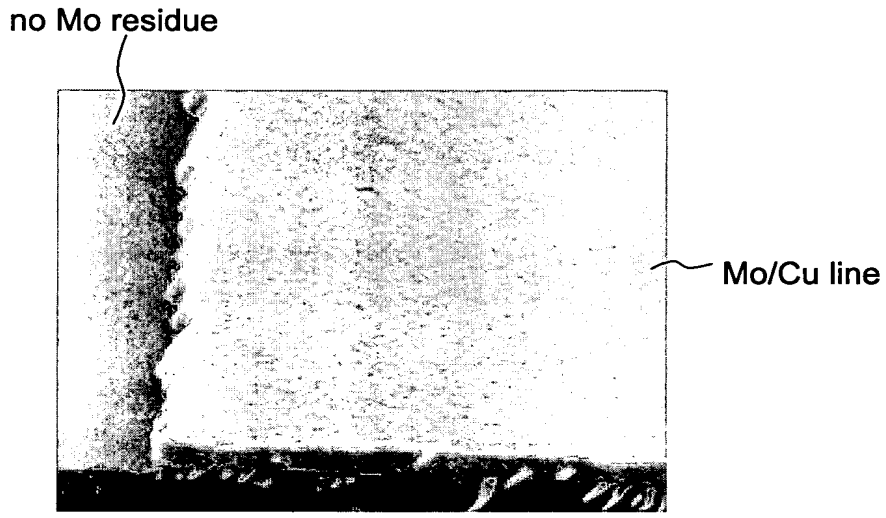

FIG. 4C

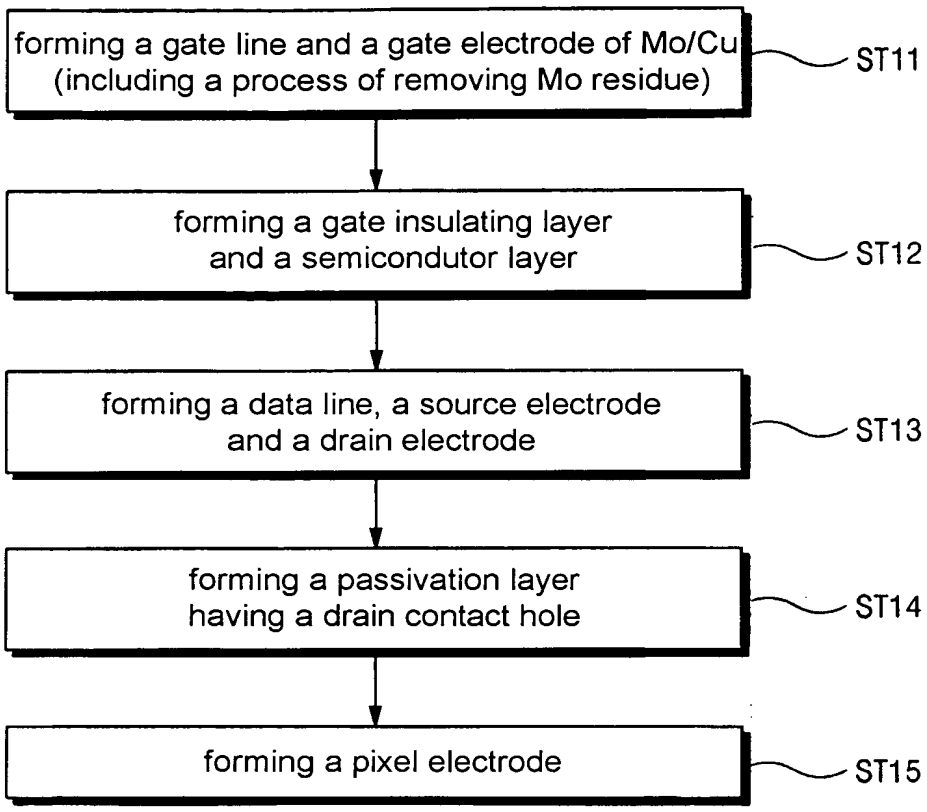
forming a gate line and a gate electrode of Mo/Cu (including a process of removing Mo residue)
ST11
forming a gate insulating layer and a semicondutor layer
ST12
forming a data line, a source electrode and a drain electrode
ST13
forming a passivation layer having a drain contact hole
ST14
forming a pixel electrode
ST15

FIG. 5